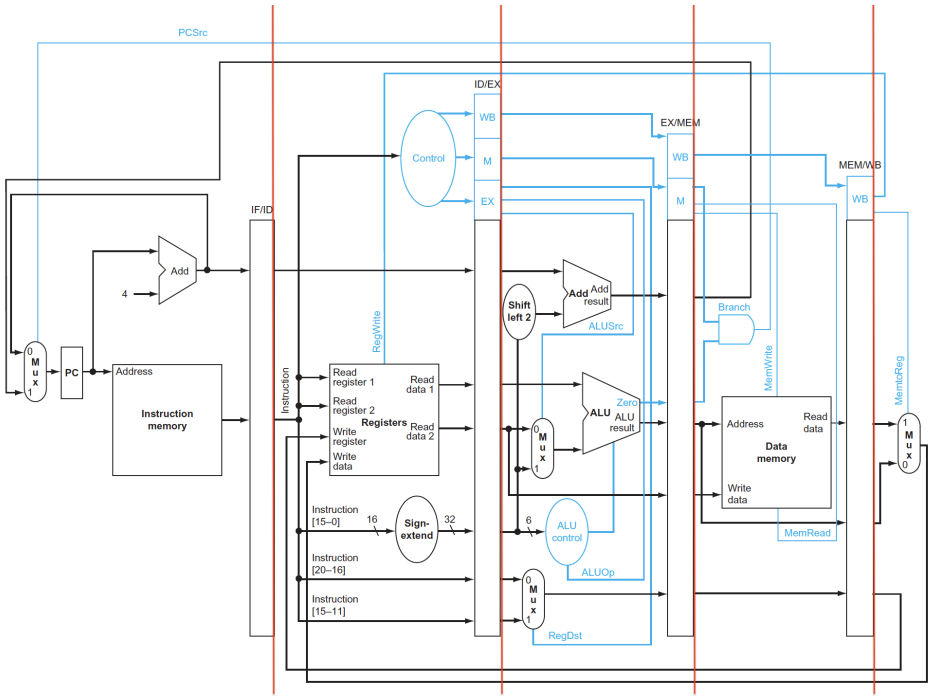
CS154 Computer Architecture
Winter Term 2019

Lab Assignment 04

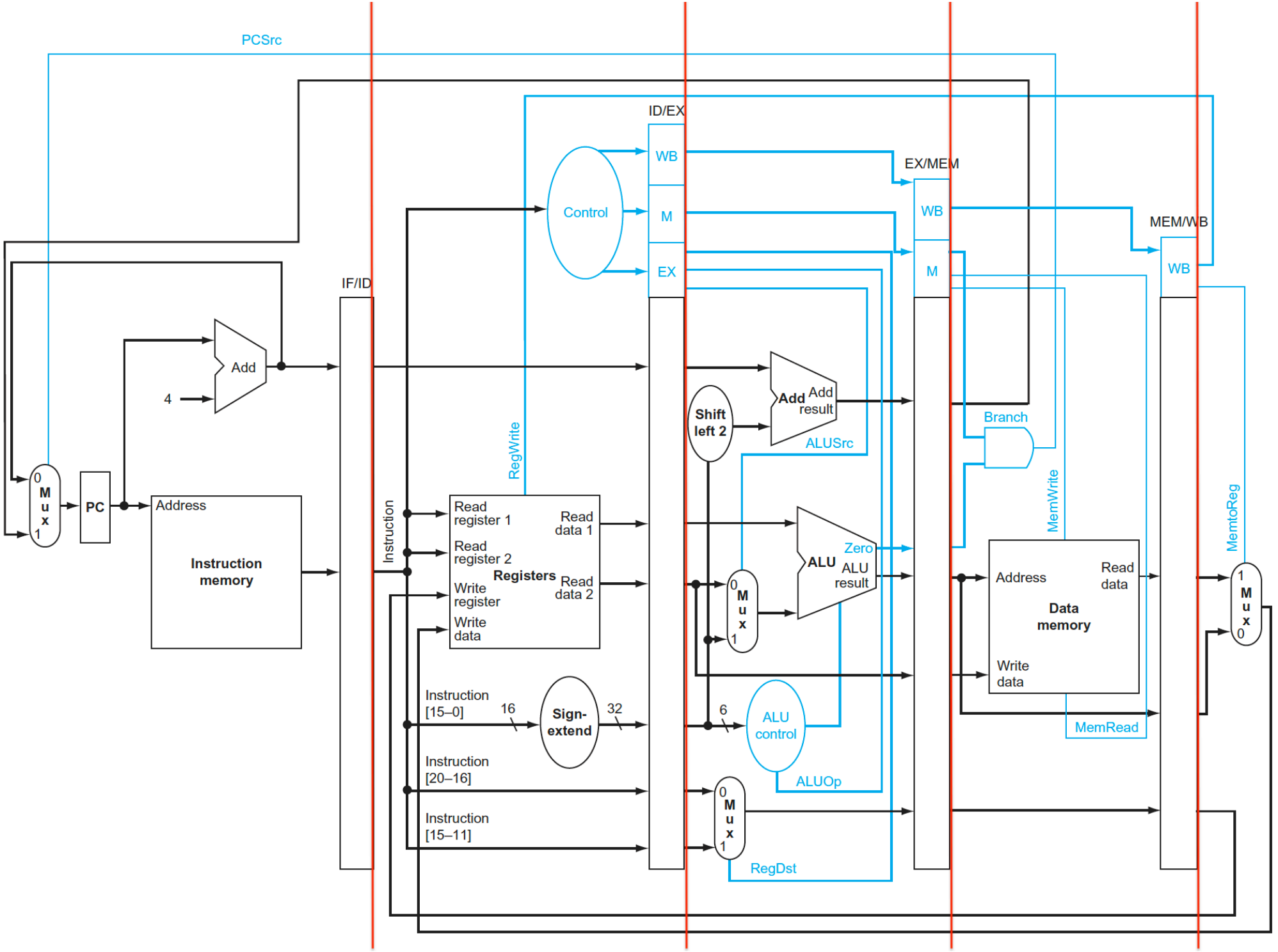
Consider the data path figure given below and in the next page:



Consider the following sequence of 7 instructions for the pipelined MIPS. Assume the pipeline is initially empty.

```
lw   $t0, 0($s0)
lw   $t1, 4($s0)
lw   $t2, 8($s0)
addi $t0, $t0, 1
add  $t1, $t1, $t2
sw   $t0, 0($s0)
sw   $t1, 4($s0)
```

Show the values of ALL data, address, and control line/bus values using this figure (you can make as many copies as needed), as the instructions follow through the stages of pipeline. Show the data and address lines more compactly using hexadecimal values. Draw a multiple-clock-cycle diagram (similar to Figure 4.52, in Page 305 on the book) to point out the cycles and units through which forwarding happens. Your grade depends on how complete the figures are in terms of the data, address, and control values, as these instructions move through the pipeline.


PCSrc
ID/EX
EX/MEM
MEM/WB
WB
M
EX
Control
IF/ID
Add
4
0
M
u
x
1
PC
Address
Instruction memory
Instruction
RegWrite
Read register 1
Read register 2
Registers
Write register
Write data
Read data 1
Read data 2
Instruction [15–0]
16
Sign-extend
32
Instruction [20–16]
Instruction [15–11]
Shift left 2
Add
Add result
ALUSrc
ALU
Zero
ALU result
6
ALU control
ALUOp
RegDst
Branch
MemWrite
MemRead
Address
Read data
Data memory
Write data
MemtoReg