THREE-LAYER WIRABILITY OF PLANAR LAYOUTS ‡

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ABSTRACT

It is well known that every planar layout is four-layer wirable. If we decrease the number of layers, there are planar layouts that cannot be wired on three layers. The problem of determining whether a planar layout is three-layer wirable is an NP-complete problem. A planar layout may be stretched vertically (horizontally) by introducing empty rows (columns). Clearly, stretching a planar layout increases its area; however, if it is stretched in certain locations it can be wired in fewer than four layers. In this paper we consider two layout stretching schemes. We present lower bounds for the worst case wiring area bounds under these two stretching schemes. We show that our lower bound for the two-layer wiring is tight and our lower bounds for three-layer wiring are not too far from known upper bounds for this problem.

I. INTRODUCTION

The *rectangle routing problem (RRP)* is a fundamental problem in VLSI design automation. As input we are given a rectangular *grid R* determined by the horizontal lines with y-coordinate values i, $0 \le i \le h + 1$ (called *tracks* or *rows*) and the vertical lines with x-coordinate values j, $0 \le j \le w + 1$ (called *columns*). The horizontal lines with y-coordinate values 0 and h + 1 and the vertical lines with x-coordinate values 0 and w + 1 form the *boundary* of R. Let $N = \{N_1, N_2, ..., N_p\}$, where each N_i is a subset of grid points on the boundary of R (excluding the corners of R), such that $N_i \cap N_j = \emptyset$ for all $i \neq j$. Each set N_i is called a *net* and its grid points are called *terminals*. We assume that there are k *conducting layers* $L_1, L_2, ..., L_k$, each is a copy of the channel grid, and L_{i+1} is considered to be laid upon L_i, $1 \le i \le k - 1$. Contacts between two layers (*vias*) can be introduced only at grid points. Under the *knock-knee* model a k-layer wiring (which is the final routing solution) is a three dimensional structure which can be characterized by two mappings: wire layout and layer assignment. A *wire layout* for a RRP is a mapping that associates each net N_i to a connected subgraph W_i of the grid R such that W_i does not share an edge with W_j for all $j \neq i$. This wire layout is called a *planar layout* or a *path disjoint layout* or simply a *layout*. We use $W = \{W_1, W_2, ..., W_p\}$ to denote the wire layout. The *layer assignment* of a planar layout is a mapping that associates each edge in W to a layer in $\{L_1, L_2, ..., L_k\}$ in such a way that for any W_i and W_j, $i \neq j$, if edges (p_1, p_2), (p_2, p_3) in W_i are assigned to L_s and L_t, respectively, and $(p_2, p_4) \in W_j$ is assigned to L_u, then $u > \max\{s, t\}$ or $u < \min\{s, t\}$. A solution for an RRP is a *k-layer wiring* formed by the composite mapping of wire layout and layer assignment. Obviously, in a wiring the segments of the same wire W_i can be connected through a via without sharing a grid point with a segment of another wire W_j in any layer. Physically speaking, in a wiring all terminals from the same net are made electrically common and no two distinct nets are connected. In practice knock-knee wirings minimize crosstalk since the area of the grid shared by two different nets is limited to grid points. A variation of the rectangle routing problem is the *channel routing problem (CRP)* in which all terminals appear on the top and bottom sides of the grid R and the objective is finding a k-layer wiring with the least number of tracks.

The above characterization of the wiring provides an approach for constructing a wiring for a CRP by finding a planar layout with least number of tracks for the given CRP and then finding a layer assignment for the layout. This approach is used by the routing algorithm for the two-terminal net CRP (each net is of size 2) by Preparata and Lipski ([PL]). The first phase of their algorithm finds a minimum-track planar layout that satisfies some special properties. In the second phase of their algorithm, the planar layout is transformed into a three-layer wiring by a powerful transformation (legal partition of the diagonal diagram induced by the planar

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layout). Their algorithm guarantees a three-layer optimal solution. Several other routing algorithms for the CRP are also based on this approach (e.g., see [PS], and [SP]).

Brady and Brown ([BB]) showed that any planar layout can be transformed into a four-layer wiring with dimensions identical to the dimensions of the planar layout. The implication of this result is that one can reduce the rectangle routing problem to the problem of finding a planar layout, since for any planar layout a four-layer wiring is always possible in the layer assignment phase. One may consider this two-phase four-layer routing approach as "standard". For example, necessary and sufficient conditions for the existence of a planar layout for the two-terminal net RRP are given in [F]. If these conditions are met, a planar layout can be found by the algorithms in [F] and [MP]. A four-layer wiring for this planar layout can be found by applying the layer assignment algorithm given in [BB]. It is not known whether the layouts generated by the algorithms in [F] and [MP] are three-layer wirable. By using the reduction given in lemma 2.1 (refer to the next section) Lipski ([Li]) gives a 19-row wire layout that is not three-layer wirable. He also shows that the problem of deciding whether a given planar layout is three-layer wirable is an NP-complete problem.

A planar layout may be *stretched vertically (horizontally)* by introducing between a pair of adjacent rows (columns) an empty row (column) (figure 3.1) without a horizontal (vertical) wire. Clearly, stretching a planar layout increases its area; however, if it is stretched in appropriate places it can be wired in fewer than four layers. Let us now investigate the trade-off between the routing area and the number of layers needed for wiring a planar layout. Let A(W) denote the area of planar layout W. The simple stretching algorithm described in [MP] generates a two-layer wiring with area not larger than 2 * A(W), by vertically stretching it between every pair of adjacent rows. In this paper we propose two different stretching schemes. Then, we show that for each of these schemes if two conducting layers are available the area bound of 2 for arbitrary planar layouts is tight, i.e. there exist planar layouts with area A(W) which cannot be stretched and wired in an area less than $(2 - \varepsilon) * A(W)$, for all $\varepsilon > 0$. Before we consider the three-layer wirability of planar layouts, we classify planar layouts into four classes according to their structure. Then, for each layout class and each stretching scheme we give lower bounds for the worst case wiring area.

II. PRELIMINARIES

In this section we review some definitions and results from [PL]. Their algorithm for finding a three-layer wiring for a given planar layout W consist of the following steps:

(i) construct the diagonal diagram D that corresponds to the layout W;
(ii) find a legal partition P of D that partitions D into two-colorable regions; and
(iii) find a layer assignment W' of W from P.

The *diagonal diagram* corresponding to the given layout is constructed as follows. At each grid point in R where W has a bend, a $(\sqrt{2}/2)$-length diagonal (called *half diagonal*) emanating from the grid point and internally bisecting the bend wire is introduced. Thus, in case there is a knock-knee at the grid point, a $\sqrt{2}$-length diagonal (called *full diagonal*), centered at the grid point, is formed. We assume that two wire segments from the same wire can form a knock-knee. One may easily transform layouts with these knock-knees and loops. We elaborate on layout transformations in the discussion section. The resulting geometric structure from this transformation is called a *diagonal diagram.* The *core* diagonal diagram of a given layout is the diagonal diagram with the half-diagonals deleted (figure 2.2). For the grid R, the partition grid G(R) is defined as follows. The *grid points* of G(R) are the points $(x + 1/2, y + 1/2)$, $0 \le x \le n$, $0 \le y \le m$. The grid points with $x = 0$, $x = n$, $y = 0$ or $y = m$ are called *boundary* points and the other points are called *internal* points. A vertical (horizontal) *grid line* in G(R) is the smallest line segment that includes all the grid points with the same y-coordinate (x-coordinate). The space between any two adjacent horizontal (vertical) grid lines is called a *row (column)* of G(R). Note that a row (column) in R is a horizontal (vertical) grid line in R, but a row (column) in G(R) is all the space between two adjacent horizontal (vertical) grid lines in G(R). The *edges* of G(R) are the segments connecting each point with its immediate neighbors, vertically, horizontally, or at 45-degree angles. It should be noted that a full diagonal in D is an edge of G(R), the end points of a full diagonal are grid points of G(R) and no two full diagonals in D cross. Let D denote the core diagonal diagram of layout W. The end points of the diagonals of D lying on nonboundary grid points of G(R) are called *vertices* of D. We say that

D has degree i, $1 \leq i \leq 4$, at vertex (s, t) if there are i full diagonals with end points at (s, t). We say that D is of *degree* i, $1 \leq i \leq 4$, if the maximum degree of any vertex in D is i; otherwise the degree of D is zero. A *legal partition* P of D (figure 2.2) is any collection of edges in G(R) satisfying the following conditions:

(a) Every internal point of G(R) is incident with an even number of edges in P;
(b) The diagonals in P are exactly the diagonals in D; and
(c) P does not contain any of the patterns shown in figure 2.1.
(dashed lines mean that the diagonal must not be present).

Forbidden patterns.
figure 2.1

The following lemma shows the significance of the notion of diagonal diagram D constructed from W and the legal partition P with respect to D.

Lemma 2.1: ([PL]): If there is a legal partition P of the core diagonal diagram D induced by the planar layout W, then there exists a three-layer assignment for W. Furthermore, a three-layer assignment for W can be easily constructed from P.

Planar Layout Core Diagonal Diagram

Legal Partition 3-Layer wiring
top layer (solid lines); middle layer (dotted lines) bottom layer (dashed lines)
figure 2.2: Examples.

We omit the description of the process for finding a layer assignment of W from a legal partition P of D. Interested readers should refer to [PL] for details. In figure 2.2 we give a layout W, its corresponding core diagonal diagram D, the legal partition P of D and the three-layer wiring for W obtained from P. In the remaining portion of this paper we use the term diagonal diagram to refer to a core diagonal diagram.

The previous lemma allows us to reduce the problem of three-layer wirability of a planar layout W to the problem of determining the existence of a legal partition P with respect to W. The crucial notion in this reduction is that of full wire layout. We say that a layout W is a *full layout* if every nonboundary edge in R is covered by a wire in W. For example, the full layout constructed from the layout in figure 2.2 is given in figure

2.3. We say that a wire layout W contains a *loop* if there is a path ((v_1, v_2), (v_2, v_3), ..., (v_{k-1}, v_k)) in W such that k > 4 and $v_1 = v_k$, where $v_1, v_2, ..., v_k$ are grid points in R. If we only consider two-terminal net full layouts (we call the full layout of this type *standard full layout*) and allow wires with loops, then there is one-to-one correspondence between standard full layouts in R and diagonal diagrams in G(R).

figure 2.3: Full layout for the planar layout given in figure 2.2.

Theorem 2.1: ([L]) A loop-free standard full wire layout W^* in R is three-layer wirable iff there exists a legal partition P of D in G(R) with respect to W^*.

III. LAYOUT STRETCHING SCHEMES

Since the problem of determining whether a planar layout is three-layer wirable is NP-complete, we investigate the problem of stretching and then wiring a planar layout. Stretching a layout vertically (horizontally) is equivalent to dividing the layout horizontally (vertically) between two adjacent rows into two sublayouts, then inserting an empty horizontal (vertical) grid line between these two sublayouts and merging the vertical (horizontal) wires in these two sublayouts at the newly introduced grid line. The following layer assignment scheme is a direct generalization of the layer assignment algorithm given in [MP].

(1) Divide W horizontally and/or vertically, into sublayouts W^1, ..., W^t, such that W^i, $1 \le i \le t$, is three-layer wirable;
(2) Find a k-layer wiring for each sublayout W^i of W;
(3) Extend the grid R to form grid R' by inserting a horizontal (vertical) empty grid line between sublayouts separated by a horizontal (vertical) dividing line introduced by step (1).
(4) Merge two adjacent sublayouts at the newly inserted grid line and introduce vias at the grid points on the new grid line if it is necessary.

Depending on the types of additional grid lines introduced, we make a distinction between the following two stretching schemes:

Scheme I: Wirings are obtained by only introducing either additional horizontal or vertical grid lines.
Scheme II: Wirings are obtained by introducing additional horizontal and vertical grid lines.

Let the height and width of grid W be h and w, respectively. The layout corresponding to the wiring obtained by the above algorithm is denoted by W'. Clearly, for Scheme I we have

$A(W') = (1+t/h) * A(W)$, (or $A(W') = (1+t/w) * A(W)$)

where t is the number of additional horizontal (or vertical) grid lines. For Scheme II we have

$A(W') = (1+t/h)*(1+u/w) * A(W)$,

where t and u are the number of additional horizontal and vertical grid lines introduced, respectively.

Stretched layouts under scheme I and II for the layout in figure 2.2(a) given in figures 3.1 (a) and 3.1 (b), respectively.

figure 3.1 (a): Layout stretched under scheme I.

figure 3.1 (b): Layout stretched under scheme II.

IV. TWO-LAYER WIRABILITY BOUNDS

In this section we discuss two-layer wirability of planar layouts. Consider the simple layouts given in figure 4.1. Both of these layouts are not two-layer wirable since one cannot assign the wire segments in these layouts so that wires from different nets do not share a grid point in one of the two available layers. Consider the full planar layout W, which has identical dimension in both directions, shown in figure 4.2. It is simple to verify that any sublayout consisting of two adjacent rows (columns) contains a sublayout with the structure shown in figure 4.1. Hence, under scheme I no less than h-1 (w-1) additional horizontal (vertical) grid lines are needed in order to obtain a two-layer wiring W'. The area of W' is $A(W') \geq (2 - 1/h)*A(W) = (2 - 1/w)*A(W)$. A straight forward generalization of the above observations is given by theorem 4.1.

Theorem 4.1: For any $\varepsilon > 0$, there exists a planar layout W such that under scheme I and II any two-layer wiring W' for it has area $A(W') > (2 - \varepsilon)*A(W)$.
Proof: For brevity the proof is omitted. □

The above theorem provide a lower bound for the worst case wiring area under scheme I and scheme II when two conducting layers are available for wiring a planar layout. In [MP] it is shown that by inserting an empty grid line between any two adjacent rows of a given planar layout, a two-layer wiring can be constructed. Therefore, the area bound 2 for wiring planar layouts under scheme I and II is best possible.

figure 4.1

figure 4.2

V. A CLASSIFICATION OF PLANAR LAYOUTS

Let $W^*(D)$ denote the set of full layouts sharing the same diagonal diagram D and $S^*(D)$ denote the standard full layout corresponding to D. From the discussion in section II we know that for a given wiring grid R, all layouts in R that share the same diagonal diagram D ($W^*(D)$) are equivalent when obtaining three-wirings through legal partitions of diagonal diagrams is concerned. Also it is easy to verify that for any diagonal diagram D if $S^*(D)$ contains a loop, so does any other full layout in $W^*(D)$. Because of this, we use the standard full layout $S^*(D)$ as the representative of $W^*(D)$.

When we explore the three-layer wirability of planar layouts, we need to consider the following two aspects of planar layouts. First, we believe that the three-layer wirability of planar layout depends on the structural complexity of layouts. For example, the layout shown in figure 4.1 is not two-layer wirable. However, it is straight forward to construct a three-layer wiring for this layout. When three-layer wiring is concerned, the structure of this layout is simple. Second, we believe that in practice there are layouts with certain structures that may never appear. For example, in a layout corresponding to a diagonal diagram of degree three or degree four there are loops. Those loops corresponding to the vertices of degree three and four in the diagonal diagram can be easily eliminated by slightly modifying the layout so that the modified diagonal diagram has degree less than 2 and the modified layout maintains the same connectivity of wires as that in the original layout.

Based on these considerations we classify layouts in a particular R by their core diagonal diagrams D into four classes:

Class (a): layouts whose core diagonal diagrams are of degree greater than two;
Class (b): layouts whose core diagonal diagrams are of degree two and the standard full layouts corresponding to their core diagonal diagrams contain loops;
Class (c): layouts whose core diagonal diagrams are of degree 2 and the standard full layouts corresponding to their core diagonal diagrams are loop-free; and
Class (d): layouts whose core diagonal diagrams are of degree one.

In the following sections we investigate the three-layer wirability under scheme I and scheme II for each of these layout classes.

VI. THREE-LAYER WIRABILITY BOUNDS FOR SCHEME I

The technique used to deriving lower bounds for the worst case wiring area under scheme I and scheme II in section IV can be generalized to handle the case when there are three conducting layers available for wiring. If we are restricted to constructing a three-layer wiring by finding a legal partition of the diagonal

diagram corresponding to the given layout, the stretching and wiring schemes given in section III can be restated as follows.

(1) Construct the core diagonal diagram D corresponding to the given layout W on the grid R;
(2) Divide D on G(R) into blocks D^1, ..., D^t, horizontally or/and vertically, by partitioning lines on grid G (accordingly layout W on R is partitioned in to sublayouts W^1, ..., W^t, such that W^i, $1 \le i \le t$, is three-layer wirable);
(3) Find legal partition P^i for each D^i and construct a three-layer wiring A^i for the sublayout W^i from P^i of D^i;
(4) Extend the grid R to form grid R' by inserting a horizontal (vertical) empty grid line between sublayouts separated by a horizontal (vertical) division line introduced in step (2).
(5) Merge two adjacent sublayouts in the division at the newly inserted grid line and introduce vias at the grid points on the new grid line if it is necessary.

figure 6.1: Strip tile arrangement A_{11}

Suppose there exists an m-row by n-column diagonal diagram D, where $1 < m < n$, for which there is no legal partition. We can construct a diagonal diagram D^* using D as a basic building block as shown in figure 6.1. It is easy to see that every m adjacent rows (columns) of D^* contains a subdiagram D. By theorem 2.1 we know that for the full layout W corresponding to D^* the area of any three-layer wiring W' obtained under scheme I satisfies $A(W') \ge (m/(m-1) - \varepsilon)*A(W)$, where $\varepsilon > 0$ can be arbitrary small when the dimension of D^* is large. Thus, one may find a lower bound for the worst case wiring area under scheme I by just finding a m-row by n-column diagonal diagram which has no legal partition. Clearly, the smaller the m value the larger the worst case area bound. We call the component diagonal diagram D of D^* a *strip tile*, and the diagonal diagram D^* constructed by using the D's as shown in figure 6.1 the *strip tile arrangement* A_{11}.

Theorem 6.1: There exist a four-row layout in layout class (a) (see figure 6.2), a five-row layout in layout class (b) (see figure 6.3), a six-row layout in layout class (c) (see figure 6.4) and a seven-row layout in layout class (d) (see figure 6.5) whose corresponding diagonal diagrams do not have legal partitions.
Proof: For brevity the proof is omitted. □

Figure 6.2

figure 6.3

figure 6.4

figure 6.5

Theorem 6.2: For any $\varepsilon > 0$ there exists a planar layout such that under scheme I any of its three-layer wirings W' obtained through legal partition of its corresponding diagonal diagram has area $A(W') > (c1 - \varepsilon) * A(W)$, where c1 is 4/3 if the layout is in class (a); c1 is 5/4 if the layout is in class (b); c1 is 6/5 if the layout is in class (c); c1 is 7/6 if the layout is in class (d);
Proof: The strip tile arrangement for all the layouts is A_{11}, except for the layout in class (c) which is the one given in figure 6.6. For the layout in class (c) one also needs to prove that there are no loops. For brevity the proof is omitted. □

Theorem 6.3: For any $\varepsilon > 0$ there exists a planar layout such that under scheme I any of its three-layer wirings W' has area $A(W') > (6/5 - \varepsilon) * A(W)$.
Proof: By Theorem 2.1 and Theorem 6.2. □

figure 6.6

VII. THREE-LAYER WIRABILITY BOUNDS FOR SCHEME II

As in the previous section, to derive lower bounds for the worst case wiring area under scheme II for each of the layout classes defined in section V, we need to find layouts with small dimensions for which legal partitions do not exist and then use these layouts to construct a larger layout with certain structure. Consider an n-row by n-column three-layer layout for which there does not exist a legal partition of its corresponding diagonal diagram. We call the diagonal diagram of such a layout a *square tile*. Let us arrange identical n-row by n-column square tiles in such a way that the lower left corner of every tile has x-coordinate i*n+j and y-coordinate j*n+i, where i and j are integers. The arrangement restricted to the rectangle formed by the horizontal lines of y-coordinate value 0 and h and vertical lines of x-coordinate values 0 and w is shown in figure 7.1. We call the arrangement restricted to this rectangle as *square tile arrangement* A_{21}. It is important to note that A_{21} is a diagonal diagram of some full planar layout.

figure 7.1:

We define a window in the arrangement A_{21} as a rectangular region with boundary lines on the horizontal and vertical grid lines of G(R). We define t(u,n) = v, for u > n, if v is the smallest integer such that in A_{21} formed by unwirable rectangles of size n by n, any u row by v column window contains at least one component square tile. The computation of t(u,n) can be performed by only considering those windows whose lower left corners are located at grid points (0, y), where $0 \le y \le n^2$. Therefore,

$$t(u, n) = \max_{y} \{ \min \{ x \mid \text{the window defined by } (0, y), (0, y+u), (x, y) \text{ and } (x, y+u) \text{ in } A_{21} \text{ contains at least one n-row by n-column square tile} \} \}$$

In any (wirable) division by scheme II, if there is a sublayout with height u there must be at least $\lfloor h/u \rfloor$ horizontal division lines and there must be at least $\lfloor w/(t(u,n)-1) \rfloor$ vertical division lines. Therefore, the area is at least $(1 + 1/u)*(1 + 1/(t(u,n)-1))*A(W)$. Without loss of generality assume w = h and $\lfloor w/(t(u,n)-1) \rfloor = w/(t(u,n)-1)$. Then, a lower bound for c_2 under scheme II, when obtaining a wiring through legal partition is considered, is given by

$$c_2 = \min\{ [1+1/u]*[1+1/(t(u, n)-1)] \mid n \le u \le n^2 \}.$$

To obtain a larger c_2 value, a smaller t(u, n) value is required; and to get a smaller t(u, n) value, smaller n value is required.

Theorem 7.1: There exist a 6-row by 6-column layout in class (a) (see figure 7.2), a 7-row by 7-column layout in class (b) (see figure 7.3), a 10-row by 10-column layout in class (c) (see figure 7.4), and a 15-row by 15-column layout in class (d) (see figure 7.5) whose corresponding diagonal diagrams do not have legal partitions.
Proof: For brevity the proof is omitted. □

Figure 7.2 Figure 7.3

Figure 7.4 Figure 7.5

Theorem 7.2: For any $\varepsilon > 0$ there exists a planar layout such that under scheme II any of its three-layer wirings W' obtained through legal partition of its corresponding diagonal diagram has area $A(W') > (c2 - \varepsilon)*A(W)$, where c2 is 1.173333 if the layout is in class (a); c2 is 1.134375 if the layout is in class (b); c2 is 1.075630 if the layout is in class (c); and c2 is 1.060950 if the layout is in class (d).
Proof: The square tile arrangement for all layout classes are A_{11}. In the tile arrangement we use square tiles of class (c) similar to the one shown in figure 7.4 to ensure that the standard full layout corresponding to the tile arrangement is loop free. For brevity the proof is omitted. □

Theorem 7.3: For any $\varepsilon > 0$ there exists a planar layout such that under scheme II any of its three-layer wirings W' has area $A(W') > (1.075630 - \varepsilon)*A(W)$.
Proof: By Theorem 2.1 and Theorem 7.2, the proof is straightforward. □

VIII. DISCUSSIONS

We considered two different layer assignment schemes for the layer assignment problem for planar layouts. We showed the lower bounds 1.20 and 1.075630 for the worst case three-layer wiring area bounds under stretching schemes I and II, respectively. The upper bound 4/3 for the approximation factors under Scheme I by using the algorithms given in [BrS] and [GZ] is close to the lower bound 1.20 developed in this paper. Using the structure of the standard full layout W, we classified planar layouts into four different classes. We considered the problem of constructing a three-layer wiring by finding a legal partition of the diagonal diagram corresponding to the stretched layout. The lower bounds we found for the approximation factors under Scheme II are much smaller than those for the Scheme I. This provides evidence that better approximation factors can be obtained under Scheme II. Under scheme I the lower bound for the worst case wiring area bound is 4/3, when a wiring constructed by finding a legal partition of the diagonal diagram corresponding to the stretched layout is concerned. This indicates that the bound 4/3 is tight unless other wiring methods are employed. Several techniques are proposed in [GZ]. We believe that the combination of the two stretching schemes considered in this paper and some wiring techniques proposed in [GZ] may result in better wiring area bounds.

IX. ACKNOWLEDGEMENT

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