Area Bound for the Three-Layer Wirings of a Class of Planar Layouts

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Abstract: It is known that the problem of determining whether or not a planar layout is three-layer wirable is NP-complete. Techniques of stretching the layouts to ensure wirability have been suggested. Lower bounds and upper bounds for the wiring area under different conditions have been developed. In this paper we show that for any $\varepsilon > 0$ there exists planar layouts with certain properties can not be stretched and three-layer wired in an area less than $(7/6 - \varepsilon)$ time of their original layout area.

I. Introduction

The channel routing problem (*CRP*) is one of the fundamental problems in VLSI design automation. As input, we are given a rectangular *grid R* (called a *channel*) determined by the horizontal lines with y-coordinate values $i, 0 \le i \le n+1$ (called *tracks*) and the vertical lines with x-coordinate values $j, 0 \le j \le m+1$ (called *columns*). The horizontal lines with y-coordinate values 0 and $n+1$ and the vertical lines with x-coordinate values 0 and $m+1$ form the *boundary* of R. Let $N = \{N_1, N_2, ..., N_p\}$, where each N_i is a subset of grid points located on the boundary of R (excluding the corner points of R), such that $N_i \cap N_j = \emptyset$ for all $i \neq j$. Each set N_i is called a *net* and the grid points in any net are called *terminals*. We assume that there are k *conducting layers* $L_1, L_2, ..., L_k$, each is a copy of the channel grid, and L_{i+1} is considered to be laid upon L_i, $1 \le i \le k-1$. Contacts between two layers (*vias*) can be introduced only at grid points. Under the *knock-knee* model a wiring (which is the final routing solution) is a three dimensional structure which can be characterized by two mappings: wire layout and layer assignment. A *wire layout* for a CRP is a mapping that associate each net N_i to a connected subgraph W_i of the grid R such that every terminal in N_i is a vertex in W_i, and W_i does not share an edge with W_j for all $i \neq j$. Such a layout is called a *path disjoint layout* (or a *planar layout*). We use $W = \{W_1, W_2, ..., W_p\}$ to denote the wire layout. The *layer assignment* of a planar layout is any mapping that associates each edge in W to a layer in $\{L_1, L_2, ..., L_k\}$ in such a way that for any W_i and W_j, $i \neq j$, if edges (p_1, p_2), (p_2, p_3) in W_i are assigned to L_s and L_t, respectively, and $(p_2, p_4) \in W_j$ is assigned to L_u, then $u > \max\{s, t\}$ or $u < \min\{s, t\}$. A wiring for a *CRP* is a composite mapping of wire layout and layer assignment. Obviously, in a wiring the segments of the same wire W_i can be connected through a via without sharing a grid point with a segment of any other wire W_j. Physically speaking, in a wiring all terminals from the same net are made electrically common and no two distinct nets are connected.

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The above characterization of the wiring provides an approach for finding a wiring for a *CRP* by finding a planar layout for the given *CRP* and then finding a layer assignment for the layout. This approach is used by the routing algorithm for the two-shore two-terminal-net *CRP* (where all terminals reside on two opposite side of R and each net is of size 2) by Preparata and Lipski ([PL]). The first phase of their algorithm finds a planar layout with some special properties. In the second phase of their algorithm, the layout is transformed into a three-layer wiring by a powerful transformation (legal partition of the diagonal diagram induced by the layout). Their algorithm guarantees a three-layer optimal solution. Several other routing algorithms are also based on this approach (e.g., see [MP], [PS], and [SP]). As shown in [BB], any planar wire layout can be transformed into a four-layer wiring. The implication of this result is that one can reduce the channel routing problem to the wire layout problem and the layer assignment problem, since for any planar layout generated in the layout phase a four-layer wiring is always possible in the layer assignment phase. One may consider this two-phase four-layer routing approach as standard. For example, in [F] the necessary and sufficient conditions of existence of a planar layout of two-terminal-net CRP (terminals can be on any side of R) were given. If these conditions are met, a planar layout can be found by the algorithms in [F] and [MP]. A four-layer wiring can be found for this planar layout by applying the layer assignment algorithm given in [BB]. It is not known whether the layouts generated by the algorithms in [F] and [MP] are three-layer wirable. By using the reduction given in theorem 2.1 (refer to the next section) Lipski ([L]) showed that there exist planar layouts that are not three-layer wirable and the problem of deciding whether a given planar layout is three-layer wirable is NP-complete.

A planar layout can be *stretched* vertically (horizontally) by introducing between a pair of adjacent rows (columns) an empty row (column) without a horizontal (vertical) wire. Clearly, stretching a planar layout increases its area; however, it it is stretched in appropriate places it can be wired in fewer than four layers. This approach was suggested by Brady, Sarrafzadeh, Gonzalez and Zheng ([BrS][GZ1]). Several layer assignment algorithms have been developed to obtain three-layer wirings with bounded area, when stretching is applied. Gonzalez and Zheng ([GZ2]) classified planar layouts into several classes. For each of these classes, they proved the lower bounds for the stretched three-layer wiring area bound under different conditions. In this paper, we consider the class of planar layouts with diagonal diagrams of degree one. We show that for any $\varepsilon > 0$ there exists planar layouts in this class such that their stretched three-layer wirings have area no less than $(7/6 - \varepsilon)$ time of their original layout area.

II. Preliminaries

In addition to the definitions given in the previous section, we need to introduce some of the basics of wiring theory. Under the knock-knee model, two wire segments in a planar layout can share a grid point of R only by either crossing each other or forming a *knock–knee* (see figure 2.1). Given a planar layout W, how to construct a three-layer wiring for it? The approach proposed in [PL] consists the following steps:

(i) construct a diagonal diagram D that corresponds to the layout W;

(ii) find a legal partition P of D that partitions D into two-colorable regions;

(iii) obtain a layer assignment A of W from P.

The diagonal diagram corresponding to the given layout is constructed as follows. At each grid point of R where W has knock-knee, introduce a $\sqrt{2}$-length *diagonal* centered at the grid point and internally bisecting the two bends that forms the knock-knee. The resulting geometric structure from this transformation is called a *diagonaldiagram*. For the grid R, the partition grid $G(R)$ is defined as follows. The grid points of $G(R)$ are the points $(x+1/2,y+1/2), 0\le x\le n, 0\le y\le m$. The grid points of $G(R)$ with $x=0, x=n, y=0$ or $y=m$ are called *boundary* points and the other points are called *internal* points. The *edges* of $G(R)$ are the segments connecting each point with its immediate neighbors, vertically, horizontally, or at 45-degree angles. It should be noticed that a diagonal in D is an edge of $G(R)$, the end points of a diagonal are grid points of $G(R)$ and no two full diagonals from D cross. Let D denote the diagonal diagram of layout W. We say that D has degree $i, 0\le i\le 4$, at point (s,t) of $G(R)$ if there are i full diagonals with end points at (s,t). We say that D is of *degree* i, $1\le i\le 4$, if the maximum degree of D at any internal point of $G(R)$ is i. A *legal partition* P of D is any collection of edges in $G(R)$ satisfying the following conditions:

(a) Every internal point of $G(R)$ is incident with an even number of edges in P;

(b) The diagonals in P are exactly the diagonals in D;

(c) P does not contain any of the patterns shown in figure 2.2.

crossing Knock-knees

Figure 2.1: knock-knees

dashed diagonals must not be present

Figure 2.2: forbidden patterns.

In [LP] it is shown that if there is a legal partition P of the diagonal diagram D induced by the layout W, then there exists a three-layer assignment for W; moreover, a three-layer wiring of W can be easily constructed from P. The existence of a legal partition of a diagonal diagram can be further equated to three-layer wirability. The crucial notion in this reduction is that of full layout. We say a layout W is a *full layout* if every nonboundary edge in R is covered by a wire in W. We say that a planar layout W

contains a *loop* if there is a path $((v_1, v_2), (v_2, v_3), ..., (v_{k-1}, v_k))$ in W such that $k > 4$ and $v_1 = v_k$, where $v_1, v_2, ..., v_k$ are grid points in R. The following theorem allows us to reduce the problem of three-layer wirability of a planar layout W to the problem of determining the existence of a legal partition P with respect to W.

Theorem 2.1 ([L]): A loop-free two-terminal-net full layout W in R is three-layer wirable if and only if there exists a legal partition P of D in $G(R)$ with respect to W; furthermore, a three-layer wiring can be easily constructed from P.

In figure 2.3 we give a layout W, its corresponding diagonal diagram D, the legal partition P of D and the three-layer wiring for W constructed from P. Note that this layout is not full and loop-free. For this example, the existence of a legal partition with respect to W is used as a sufficient condition for the three-layer wiring of W. Using theorem 2.1, Lipski ([L]) showed that the problem of determining whether or not a given planar layout is three-layer wirable is NP-complete. It should be mentioned this theorem is a restricted version of the general theorem on the wirability of planar layouts given in [LP]. For more details on the wiring theory, refer to [LP].

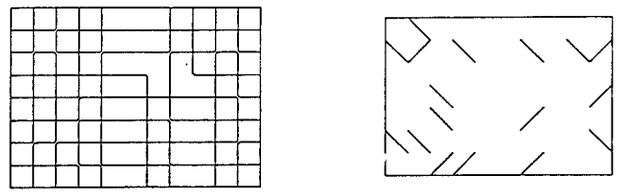


Figure 2.3: examples.

Since that the problem of finding a three-layer wiring for a given layout W is very unlikely polynomial time solvable, it is suggested in [BrS] and [GZ1] that instead of finding a three-layer wiring for W, one can stretch W to obtain a new layout W' and then find a three-layer wiring for W'. Stretching a layout vertically (horizontally) is equivalent to dividing the layout horizontally (vertically) between two adjacent rows into two sublayouts, then inserting an empty horizontal (vertical) grid line between these two

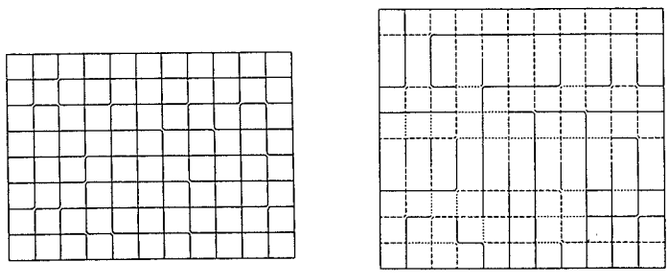
sublayouts and merging the vertical (horizontal) wires in these two sublayouts at the newly introduced grid line. The following layer assignment scheme is a direct generalization of the layer assignment algorithm given in [MP].

(1) Divide W horizontally (vertically) into sublayouts W^1, ..., W^t, such that W^i, $1 \le i \le t$, is three-layer wirable;

(2) Find a three-layer wiring for each sublayout W^i of W;

(3) Extend the grid R to form grid R' by inserting a horizontal (vertical) empty grid line between sublayouts separated by a horizontal (vertical) dividing line introduced by step (1).

(4) Merge two adjacent sublayouts at the newly inserted grid line and introduce vias at the grid points on the new grid line if it is necessary.



(a) (b)

Figure 2.4:stretching and wiring.

Let the height and width of layout W be h and w, respectively. Let the layout obtained from W by stretching be denoted by W'. We use $A(.)$ to denote the area of a layout. Then,

$$A(W')=(1+t/h)*A(W), \text{ (or } A(W')=(1+t/w)*A(W) \text{)}$$

where t is the number of additional horizontal (or vertical) grid lines. As an example, from the layout in figure 2.4 (a) one can obtain a wiring shown in figure 2.4 (b) by the stretching and wiring method.

III. The Result

Our approach to deriving lower bound for the wiring area of planar layout under the stretching scheme discussed in the previous section consists of two parts: first, we need to find a three-layer unwirable layout W' with minimum number of rows; then we use this layout as a basic building block to construct a layout W such that almost every fixed number of rows of W is not three-layer wirable. By theorem 2.1, we only need to consider loop-free two-terminal-net full layout, and the wirability of such a layout can be determined by inspecting whether or not the diagonal diagram of the layout admits a legal partition.

To simplify our proof, we use the following conventions. We use the ordered pair (x, y) to refer to the grid point of $G(R)$ with coordinate values x and y. A horizontal or vertical line connecting (x_1, y_1) and (x_2, y_2) is referred to by $[(x_1, y_1), (x_2, y_2)]$. We use the notion "$S_1 \rightarrow S_2 \rightarrow ... \rightarrow S_k$" to mean that "statement S_1 holds; since S_1 holds, then S_2 holds; since $S_1, S_2, ..., S_{k-1}$ hold, then S_k holds". Let P' be a set of horizontal and vertical line segments in $G(R)$. In what follows we say that an internal grid point v of $G(R)$ is legally connected by the segments in P' if the sum of the number of diagonals from D and the number of line segments from P' incident with v is even, and there are no forbidden patterns that include v. Clearly, $P' \cup$ {all diagonals in D} is a legal partition of D if and only if all internal grid points are legally connected by the line segments in P'. The following lemma is useful for simplifying our proofs.

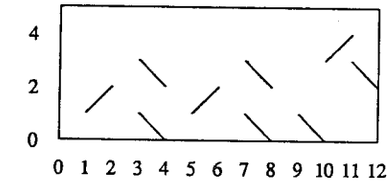


Figure 3.1

Lemma 3.1: The diagonal diagram give in figure 3.1 does not admit any legal partition which contains a horizontal partitioning line with point (11, 4) as its right end point.

Proof : Refer to [GZ3] for the details.

□

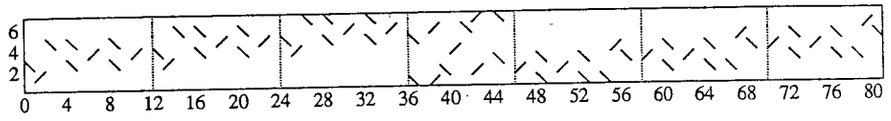


Figure 3.2 (a): strip tile

We use the diagonal diagram of figure 3.1 as a *basic component* to construct a diagonal diagram shown in figure 3.2 (a). The dotted lines in this figure seperate the basic components in the diagram.

Lemma 3.2: The diagonal diagram given in figure 3.2 (a) does not admit any legal partition.

Proof: The proof is by contradiction. Suppose it has a legal partition P. By using arguments similar to the ones at the beginning of proof of lemma 6.4 one can show that we only need to consider the following two cases.

case 1: There is a horizontal partitioning line, a, in P with (41,4) as its left end point (figure 3.2 (b)). This horizontal line and the diagonal diagram satisfies the conditions of lemma 3.1. Therefore, P is not a legal partition (figure 3.2 (b)). This contradicts the assumption that P is a legal partition.

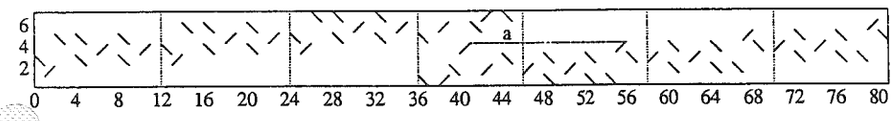


Figure 3.2 (b): case 1.

case 2: There is a vertical partitioning line, a, in P with (41,4) as its bottom end point (figures 3.2 (c), (d) and (e)).

There are two subcases need to be considered, depending on how vertex (42,5) is legally connected in P.

subcase 2.1: Vertex (42,5) is the left end point of a horizontal partitioning line, b, in P (figures 3.2 (c)). The horizontal line and the diagonal diagram satisfies the conditions of lemma 3.1. Therefore there cannot be a legal partition for the diagonal diagram given in figure 3.2 (a) (figure 3.2 (c)). This contradicts the assumption that P is a legal partition.

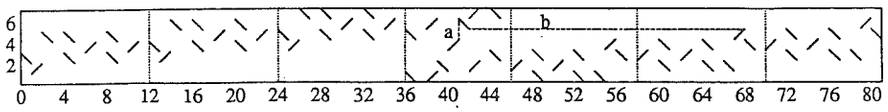


Figure 3.2 (c): subcase 2.1

subcase 2.2: Vertex (42,5) is the top end point of vertical partitioning line, b, in P (figures 3.2 (d) and (e)).

There are two subcases need to be considered, depending on how vertex (43,2) is legally connected in P.

subcase 2.2.1: Vertex (43,2) is the bottom end point of a vertical partitioning line, c, in P (figure 3.2 (d)).

When this vertical line is in P, vertex (42,6) cannot be legally connected in P (figure 3.2 (d)). This contradicts the assumption that P is a legal partition.

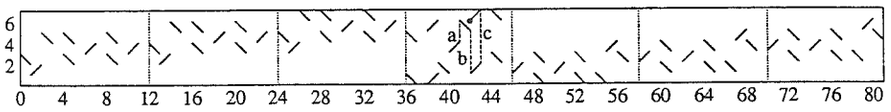


Figure 3.2 (d): subcase 2.2.1.

subcase 2.2.2: Vertex (43,2) is the left end point of a horizontal partitioning line, c, in P (figure 3.2 (e)).

b = [(42,1),(42,5)] and c = [(43,2),(45,2)] are in $P \rightarrow d$ = [(44,3),(44,7)] is in $P \rightarrow e$ = [(45,6),(80,6)] is in $P \rightarrow$ the conditions of lemma 3.1 (figure 3.2 (e)). This contradicts the assumption that P is a legal partition.

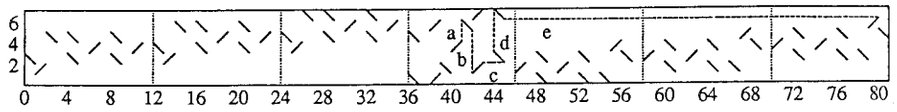


Figure 3.2 (e): subcase 2.2.2.

Since P does not satisfy any of the cases, it must be that there is no legal partition for the diagonal diagram D given in figure 3.2 (a).

□

Theorem 3.1: There exists a seven-row three-layer unwirable layout with diagonal diagram of degree 1.
Proof: The existence of such layout follows from lemma 3.2, the fact that the two-terminal-net full layout for the diagonal diagram given by figure 3.2 (a), which has degree 1, is loop-free (see figure 3.3), and theorem 2.1.

□

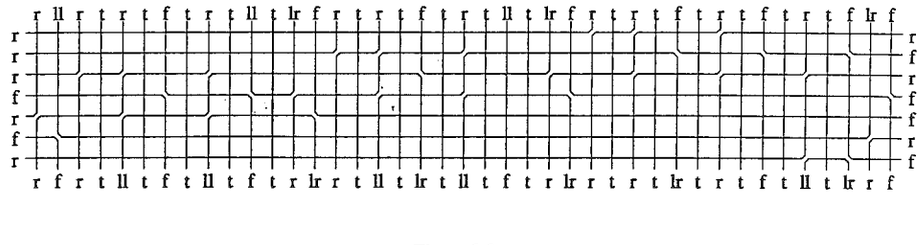


Figure 3.3

Let us look at the two-terminal-net full layout W corresponding to the diagonal diagram given in figure 3.2 (a) more closely. We call a net in W with two terminals (x_1, y_1) and (x_2, y_2) a *rising net* if its two terminal are not located on the same boundary side of R, $x_1 < x_2$ and $y_1 < y_2$; a *falling net* if its two terminals are not located on the same boundary side of R, $x_1 < x_2$ and $y_1 > y_2$; a *through net* if its two terminals are not located on the same boundary side of R, $x_1 = x_2$ or $y_1 = y_2$; a *local net* if its two terminals are located on the the same boundary side of R. Clearly each net in the two-terminal-net full layout corresponding to the diagonal diagram in figure 3.2 (a) is of (exactly) one of these four types. We label each terminal with r,f,t or l depending on the type of net the terminal belong to. For two terminals belong to the same local net and located at a horizontal boundary side, we call the one with the smaller x-coordinate value the *left terminal of the net* and the other the *right terminal of the net*. We use ll and lr to distinguish left terminals and right terminals of local nets with terminals located on the top and bottom boundary sides of R. The diagonal diagram given in figure 3.2 (a) consists of 7 rows and 81

columns, and it is symmetric with respect to the diagonal located at the 4-th row and 41st column. Figure 3.3 shows the two-terminal-net full layout corresponding to the diagonal diagram formed by the 41 leftmost columns of the diagonal diagram given in figure 3.2 (a) with all terminals labeled. It is easy to see that every wire (for a net) in this layout is *vertically monotone*, i.e. a vertical line located between any two adjacent columns of R does not intersect any wire more than once.

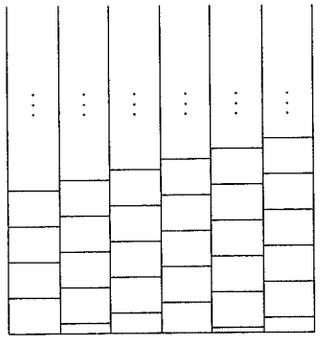


Figure 3.4: tile arrangement A_1.

Let us call the diagonal diagram given in figure 3.2 (a) as a *strip tile* and the lower left corner point of the partition grid $G(R)$ be (0, 0). By placing a 7-row by 81-column strip tile in $G(R)$ such that (i*81, i*2+j*7), where $0 \le i \le 6$ and $j \ge 0$, we obtain a tile arrangement shown in figure 3.4. We call this arrangement as *strip tile arrangement* A_1. The two-terminal-net full layout corresponding to A_1 is divided into three-layer unwirable sublayouts with diagonal diagram shown in figure 3.2 (a) by division lines, which are the boundary of tiles, in the tile arrangement A_1. Thus, a horizontal (vertical) division line can be treated as the top (left) boundary of one sublayout and the bottom (right) boundary of another sublayout. Consequently, the crossing point of a wire and a division line in A_1 can be treated as a terminal of both adjacent sublayouts along the division line. We may call such a crossing point as a *pseudo terminal*. Consider any two adjacent strip tiles T^1 and T^2 in A_1. Let the two-terminal-net full layouts corresponding to them be W^1 and W^2, respectively. If T^2 is on top of T^1, then any pseudo terminal v of W^1 on the top boundary side of W^1 is a pseudo terminal of W^2 on the bottom boundary side of W^2. Obviously, a vertical wire of a through net in a sublayout corresponding to a tile in A_1 is a wire segment of a vertical wire going through the two-terminal-net full layout corresponding to A_1. We can ignore these vertical wires since they are never parts of a loop. It is easy to see that if v is labeled f or ll in W^1 then v is labeled f or lr in W^2; and if v is labeled r or lr in W^1 then v is labeled r or ll in W^2. In the case that T^1 is to the left of T^2, any pseudo terminal v of W^1 on the right boundary side of W^1 is a pseudo terminal of W^2 on the left boundary side of W^2. Then, if v has the same label in both W^1 and W^2. From these observations, one can easily conclude that every wire in the two-terminal-net full layout corresponding to the arrangement A_1 is vertically monotone (a more formal proof for this is given in

[GZ3]). It is easy to see that A_1 is of degree 1, we have

Lemma 3.3: The tile arrangement A_1 is of degree 1 and the two-terminal-net full layout corresponding to A_1 is loop-free.

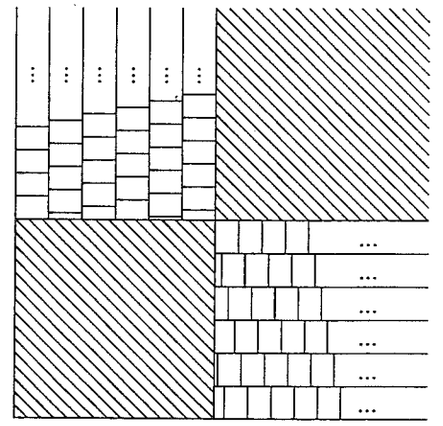


Figure 3.5: tile arrangement A_2

Let us construct a tile arrangement A_2 by using the arrangement A_1 as shown in figure 3.5. The shadowed area in this tile arrangement contains no diagonals. By lemma 3.3, we have

Lemma 3.4: The tile arrangement A_2 is of degree 1 and the two-terminal-net full layout corresponding to A_2 is loop-free.

□

Theorem 3.2: For any small $\varepsilon > 0$ there exists a planar layout W whose diagonal diagram is of degree 1 and any three-layer wiring of layout W' obtained by vertically or horizontally stretching W has area $A(W') > (7/6 - \varepsilon) * A(W)$.

Proof: Consider the two-terminal-net full layout W corresponding to the tile arrangement of A_2. By lemma 3.4 we know that A_2 is of degree 1 and W is loop-free. In this layout, except for 7*81 rows and 7*81 columns, every seven adjacent rows or columns is not three-layer wirable since it contains a two-terminal-net full sublayout with a diagonal diagram shown in figure 3.2 (a), which does not admit any legal partition, by lemma 3.2. Since $A(W') = (1+t/h) * A(W)$, (or $A(W') = (1+t/w) * A(W)$), where t is the number of additional horizontal (or vertical) grid lines introduced when stretching, and the dimension of this layout can be arbitrarily large, i.e. the value of t can be as large as $h/6$ (or $w/6$), we have our conclusion.

□

IV. Discussions

We considered the three-layer wirability problem for planar layouts under a layout transformation called stretching. We showed that for any $\varepsilon > 0$, there exists planar layouts W which cannot be stretched under stretching scheme I such that the resulting layout W' is three-layer wirable and $A(W') > (7/6-\varepsilon) * A(W)$. In [GZ1], it is shown any layout W with diagonal diagram of degree 1 can be stretched to obtain a layout W' such that it can be wired in three conducting layers in area $A(W') < (5/4) * A(W)$. We conjecture that there does not exists a 6-row loop-free two-terminal-net full planar layout with a diagonal diagram of degree 1. This conjecture strongly implies that our 7/6 lower bound for the three-layer wiring area bound for the class of planar layouts with diagonal diagrams of degree 1 is tight by using our stretching method. It should be mentioned that other results on the upper bound and lower bounds of the area of three-layer wirings of other layout classes are given in [GZ1], [GZ2] and [GZ3]. In [Z], a more general form of layout transformation is proposed and three-layer wirability of the layouts under this layout transformation is discussed. It was conjectured in [Z] that under the proposed layout transformations every planar layout is three-layer wirable without introducing additional area. However, even this conjecture can be proven to be true, the problem of finding such a transformation can be very difficult. Thus, combining the stretching and other layout transformations may provide a feasible approach to the task of designing efficient layer assignment algorithms which may result in three-layer wirings with small area.

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