LAYER ASSIGNMENT FOR PLANAR LAYOUTS‡

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ABSTRACT

It is well known that every planar layout is four-layer wirable. If we decrease the number of layers, there are planar layouts that cannot be wired on three layers. The problem of determining whether a planar layout is three-layer wirable is an NP-complete problem. A planar layout may be stretched vertically (horizontally) by introducing empty rows (columns). Clearly, stretching a planar layout increases its area; however, if it is stretched in certain locations it can be wired in fewer than four layers. It is well known that every planar layout W can be stretched and two-layer wired in an area not larger than twice the area of W. The bound on the wiring area has been shown to be best possible, i.e., there are planar layouts that need to be stretched by this factor of two. In this paper, we investigate the problem of stretching and then wiring in three layers a planar layout. We show that the additional area required is no more than 1/3 of the planar layout area. We also show that for a class of planar layouts, the additional area is not more than 1/4 of the the planar layout area.

I. INTRODUCTION

The *rectangle routing problem (RRP)* is a fundamental problem in VLSI design automation. As input we are given a rectangular *grid R* determined by the horizontal lines with y-coordinate values i, $0 \leq i \leq n + 1$ (called *tracks* or *rows*) and the vertical lines with x-coordinate values j, $0 \leq j \leq m + 1$ (called *columns*). The horizontal lines with y-coordinate values 0 and n + 1 and the vertical lines with x-coordinate values 0 and m + 1 form the *boundary* of R. Let $N = \{N_1, N_2, ..., N_p\}$, where each N_i is a subset of grid points on the boundary of R (excluding the corners of R), such that $N_i \cap N_j = \emptyset$ for all $i \neq j$. Each set N_i is called a *net* and its grid points are called *terminals*. We assume that there are k *conducting layers* $L_1, L_2, ..., L_k$, each is a copy of the channel grid, and L_{i+1} is considered to be laid upon L_i, $1 \leq i \leq k - 1$. Contacts between two layers (*vias*) can be introduced only at grid points. Under the *knock-knee* model a k-layer wiring (which is the final routing solution) is a three dimensional structure which can be characterized by two mappings: wire layout and layer assignment. A *wire layout* for a RRP is a mapping that associates each net N_i to a connected subgraph W_i of the grid R such that W_i does not share an edge with W_j for all $j \neq i$. This wire layout is called a *planar layout* or a *path disjoint layout* or simply a *layout*. We use $W = \{W_1, W_2, ..., W_p\}$ to denote the wire layout. The *layer assignment* of a planar layout is a mapping that associates each edge in W to a layer in $\{L_1, L_2, ..., L_k\}$ in such a way that for any W_i and W_j, $i \neq j$, if edges (p_1, p_2), (p_2, p_3) in W_i are assigned to L_s and L_t, respectively, and $(p_2, p_4) \in W_j$ is assigned to L_u, then $u > \max\{s, t\}$ or $u < \min\{s, t\}$. A solution for an RRP is a *k-layer wiring* formed by the composite mapping of wire layout and layer assignment. Obviously, in a wiring the segments of the same wire W_i can be connected through a via without sharing a grid point with a segment of another wire W_j in any layer. Physically speaking, in a wiring all terminals from the same net are made electrically common and no two distinct nets are connected. In practice knock-knee wirings minimize crosstalk since the area of the grid shared by two different nets is limited to grid points. A variation of the rectangle routing problem is the *channel routing problem (CRP)* in which all terminals appear on the top and bottom sides of the grid R and the objective is finding a k-layer wiring with the least number of tracks.

The above characterization of the wiring provides an approach for constructing a wiring for a CRP by finding a planar layout with least number of tracks for the given CRP and then finding a layer assignment for the layout. This approach is used by the routing algorithm for the two-terminal net CRP (each net is of size 2) by Preparata and Lipski ([PL]). The first phase of their algorithm finds a minimum-track planar layout that satisfies some special properties. In the second phase of their algorithm, the planar layout is transformed into a three-layer wiring by a powerful transformation (legal partition of the diagonal diagram induced by the planar layout). Their algorithm guarantees a three-layer optimal solution. Several other routing algorithms for the CRP are also based on this approach (e.g., see [PS], and [SP]).

Brady and Brown ([BB]) showed that any planar layout can be transformed into a four-layer wiring with dimensions identical to the dimensions of the planar layout. The implication of this result is that one can reduce the rectangle routing problem to the problem of finding a planar layout, since for any planar layout a four-layer wiring is always possible in the layer assignment phase. One may consider this two-phase four-layer routing approach as "standard". For example, necessary and sufficient conditions for the existence of a planar layout for the two-terminal net RRP are given in [F]. If these conditions are met, a planar layout can be found by the algorithms in [F] and [MP]. A four-layer wiring for this planar layout can be found by applying the layer assignment algorithm given in [BB]. It is not known whether the layouts generated by the algorithms in [F] and [MP] are three-layer wirable.

By using the reduction given in lemma 2.1 (refer to the next section) Lipski ([Li]) gives a 19-row wire layout that is not three-layer wirable. He also shows that the problem of deciding whether a given planar layout is three-layer wirable is an NP-complete problem.

A planar layout may be *stretched vertically (horizontally)* by introducing between a pair of adjacent rows (columns) an empty row (column) without a horizontal (vertical) wire. Clearly, stretching a planar layout increases its area; however, if it is stretched in certain places it can be wired in fewer than four layers. Let us now investigate the trade-off between the routing area and the number of layers needed for wiring a planar layout. Let A(W) denote the area of planar layout W. The simple stretching algorithm described in [MP] generates a two-layer wiring with area not larger than 2 * A(W), by vertically stretching it between every pair of adjacent rows. In [GZ] it is shown that there exist planar layouts with area A(W) which cannot be stretched and wired in an area less than $(2 - \epsilon)$ * A(W), for all $\epsilon > 0$. Therefore, the area bound for arbitrary planar layouts is tight, if we are only allowed to

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vertically or horizontally stretch the planar layout. For any given planar layout W, one can find a four-layer wiring with area A(W) [BB]. What is the area trade-off for three layers? In this paper we show that any planar layout W can be stretched and three-layer wired on an area not larger than (4/3) * A(W). Our technique consists of vertically stretching a planar layout every three rows. We show that each of these 3-row planar layouts is three-layer wirable. Gonzalez and Zheng [GZ] show that there are planar layouts with the property that any four adjacent rows or columns in it are not three-layer wirable. Therefore, our 4/3 bound is best possible for arbitrary layouts if we are only allowed to vertically or horizontally stretch the planar layouts. Gonzalez and Zheng [GZ] classify planar layouts according to their structure. For each layout class they give a constant c such that there is a c-row planar layout that is not three-layer wirable. In this paper we also show that every planar layout in the simplest class of planar layouts defined in [GZ] (this class includes all planar layouts with diagonal diagrams of degree one [refer to next section]) can be stretched and three-layer wired on an area not larger than 1.25 * A(W). This constant is close to the lower bound of 7/6 given in [GZ] for this class of planar layouts.

In section II we present some preliminary definitions and results introduced by Preparata and Lipski [PL] to study three-layer wirings. Our stretching-wiring algorithm is given in section III. In section IV we show that every three-row planar layout is three-layer wirable. In section V we present an algorithm that generates three-layer wirings for a special class of four-row planar layouts. In section VI we discuss the implications of our results.

II. PRELIMINARIES

In this section we review some definitions and results from [PL]. Their algorithm for finding a wiring for a given planar layout W consist of the following steps:

(i) construct the diagonal diagram D that corresponds to the layout W;

(ii) find a legal partition P of D that partitions D into two-colorable regions; and

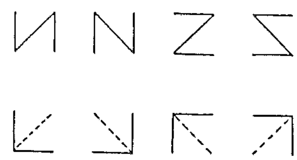
(iii) find a layer assignment W' of W from P.

The *diagonal diagram* corresponding to the given layout is constructed as follows. At each grid point in R where W has a bend, a ($\sqrt{2}/2$)-length diagonal (called *half diagonal*) emanating from the grid point and internally bisecting the bend wire is introduced. Thus, in case there is a knock-knee at the grid point, a $\sqrt{2}$-length diagonal (called *full diagonal*), centered at the grid point, is formed. The resulting geometric structure from this transformation is called a *diagonal diagram.* The *core* diagonal diagram of a given layout is the diagonal diagram with the half-diagonals deleted (see figure 2.2). For the grid R, the partition grid G(R) is defined as follows. The *grid points* of G(R) are the points (x + 1/2, y + 1/2), 0 $\leq$ x $\leq$ n, 0 $\leq$ y $\leq$ m. The grid points with x = 0, x = n, y = 0 or y = m are called *boundary* points and the other points are called *internal* points. A vertical (horizontal) *grid line* in G(R) is the smallest line segment that includes all the grid points with the same y-coordinate (x-coordinate). The space between any two adjacent horizontal (vertical) grid lines is called a *row (column)* of G(R). Note that a row (column) in R is a horizontal (vertical) grid line in R, but a row (column) in G(R) is all the space between two adjacent horizontal (vertical) grid lines in G(R). The *edges* of G(R) are the segments connecting each point with its immediate neighbors, vertically, horizontally, or at 45-degree angles. It should be noted that a full diagonal in D is an edge of G(R), the end points of a full diagonal are grid points of G(R) and no two full diagonals in D cross. Let D denote the core diagonal diagram of layout W. The end points of the diagonals of D lying on nonboundary grid points of G(R) are called *vertices* of D. We say that D has degree i, 1 $\leq$ i $\leq$ 4, at vertex (s, t) if there are i full diagonals with end points at (s, t). We say that D is of *degree* i, 1 $\leq$ i $\leq$ 4, if the maximum degree of any vertex in D is i; otherwise the degree of D is zero. A *legal partition* P of D (see figure 2.2) is any collection of edges in G(R) satisfying the following conditions:

(a) Every internal point of G(R) is incident with an even number of edges in P;

(b) The diagonals in P are exactly the diagonals in D; and

(c) P does not contain any of the patterns shown in figure 2.1. (dashed lines mean that the diagonal must not be present).



Forbidden patterns.
figure 2.1

The following lemma shows the significance of the notion of diagonal diagram D constructed from W and the legal partition P with respect to D.

Lemma 2.1. ([PL]): If there is a legal partition P of the core diagonal diagram D induced by the planar layout W, then there exists a three-layer assignment for W. Furthermore, a three-layer assignment for W can be easily constructed from P.

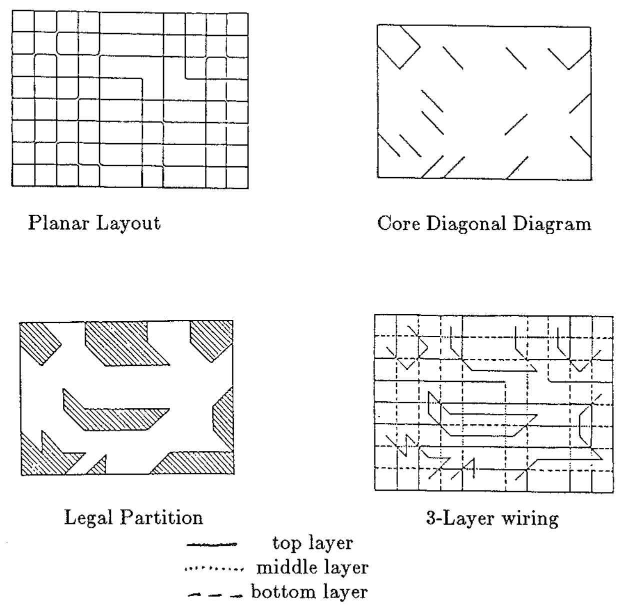


figure 2.2: Examples.

We omit the description of the process for finding a layer assignment of W from a legal partition P of D. Interested readers should refer to [PL] for details. In figure 2.2 we give a layout W, its corresponding core diagonal diagram D, the legal partition P of D and the three-layer wiring for W obtained from P. In the remaining portion of this paper we use the term diagonal diagram to refer to a core diagonal diagram.

III. FINDING STRETCHING POSITIONS

As mentioned in section I, one can always find a wiring for a given planar layout by stretching it. Stretching a planar layout vertically is equivalent to inserting into the layout a grid line without any horizontal wires on it. Let us now briefly describe our three-layer wiring approach. First we divide a planar layout horizontally into three-layer wirable sublayouts. Then we find a three-layer wiring for each of these sublayouts and insert an empty grid line between every pair of adjacent sublayouts. In the final step, the vertical wires in every two adjacent sublayouts are joined at the newly introduced grid line between them by vias whenever necessary. Since the problem of determining whether or not a planar layout is three-layer wirable is NP-complete [Li], it is simple to show that the problem of finding a minimum area 3-layer wiring of a given layout W by stretching it is NP-hard. Our problem consists of dividing vertically a planar layout into a small number of sublayouts such that each of these sublayouts can be wired by some given algorithm.

In section IV we present algorithm 3ROW-ASSIGN that constructs a three-layer wiring for any 3-row planar layout. Given any planar layout, it can be vertically stretched every three rows. Each of these three-row sublayout is three-layer wirable by algorithm 3ROW-ASSIGN. Therefore for an arbitrary planar layout W one can stretch and three-layer wire it on an area not larger than (4/3) * A(W). In section V we present algorithm 4ROW-ASSIGN that constructs a three-layer wiring for any four-row planar layout whose diagonal diagram is of degree 1. Similarly if the diagonal diagram of a given planar layout W is of degree 1, algorithm 4ROW-ASSIGN can be used to obtain a three-layer wiring with area not larger than (5/4) * A(W).

Given a planar layout W whose diagonal diagram is of degree greater than 1, can we find a three-layer wiring with area smaller than (4/3) * A(W)? The answer to this question is affirmative. An algorithm to accomplish this uses the algorithm mentioned above on different parts of the layout. For more details see [GZ1].

IV. A LAYER ASSIGNMENT ALGORITHM FOR THREE-ROW PLANAR LAYOUTS.

Our layer assignment algorithm for a three-row planar layout W is based on finding a legal partition P of the diagonal diagram D. This legal partition is obtained from a legal connection C of the vertex diagram V induced by D. The *vertex diagram* V is constructed from D as follows: if D has odd degree at nonboundary grid point (s, t) of G(R), we assign a vertex to point (s, t); otherwise there is no vertex at grid point (s, t). A *legal connection* C of V is a set of horizontal and vertical grid line segments of G(R) that satisfies the following conditions:

(i) The end point of any line segment must either lie on the boundary of G(R) or be incident to a vertex of V;
(ii) For every vertex v in V there is exactly one horizontal or vertical line segment incident to v;
(iii) There are no two line segments l' and l'' in C lying on two adjacent vertical (horizontal) grid lines of G(R) such that their projections to the y axis (x axis) share more than one point;
(iv) No two orthogonal line segments in C intersect.

From the definition of legal partition and legal connection, it is easy to prove the following lemma.

Lemma 4.1: If C is a legal connection of vertex diagram V induced by the diagonal diagram D, then superimposing C on D yields a legal partition of D.

□

By this lemma, the problem of finding a legal partition P of D is reduced to the problem of finding a legal connection C of V induced by D. We graphically represent all vertices in V by solid dots and all internal grid points of G(R) which are not vertices of V by circles. There are two internal horizontal grid lines in G(R). If we partition the vertices in V into *columns* according to the vertical grid lines of G(R) where they are located, we have four different types of columns. The legal connection C of V is constructed column by column in a left-to-right scan of V. When a column is being considered, we need to remember the connection of the preceding column. Based on the configuration of this column and the type of the current column, the connection of the current column is determined. The connection of the current column may modify the connection of the immediately preceding column; however this modification guarantees that the resulting connection is legal. Without loss of generality we assume that the left and right boundary of G(R) are columns with no vertices.

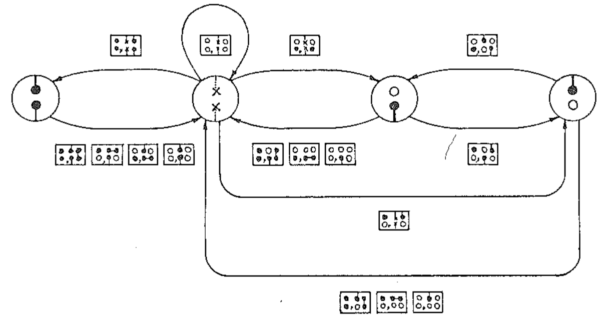
procedure *3-ROW-ASSIGN*
(1) Construct the diagonal diagram D from W;
(2) Construct the vertex diagram V corresponding to the diagonal diagram D;
(3) Construct a legal connection C for V as follows:
for c ← 1 to n **do** /* left and right sides of G(R) are columns 0 and n+1, respectively */
begin
Depending on the type of column c and the connection of column c - 1 make a legal connection by using the actions given by the finite automata depicted in figure 4.1 (which is explained in the following paragraph) for the vertices in columns c and c - 1. Note that this step might modify the connection of column c - 1 obtained in the previous iteration.
end
(4) Construct the legal partition P of D from the legal connection C of V obtained in step (3) and build a three-layer wiring of W from P.
end of 3-ROW- ASSIGN

The actions in step (3) of the algorithm can be visualized by means of a finite state automata. The transition diagram for this automata is illustrated in figure 4.1. Each state corresponds to the connection in the previous column. The state composed of two x's means that those grid points could have a vertex or not, and the dotted lines mean that those lines are not present. Associated with each transition in the automaton we define an input-output pair. The first component of the pair, the input, specifies the type of the column being considered and the second component, the output, shows the final configuration for both the previous and the current columns. By starting in the state corresponding to the left boundary of G(R), it is easy to prove by induction that a legal connection C of V is constructed. Therefore, we have the following theorem.

Theorem 4.1 Algorithm 3-ROW-ASSIGN generates a legal connection for any three-row planar layout in O(n) time, where n is the number of columns in R.
Proof: For brevity the proof is omitted.

□

An example of a diagonal diagram D with vertex diagram V is given in figure 4.2. A legal connection C obtained by our algorithm and the legal partition P of D by superimposing C on D is also



Finite Automaton
Figure 4.1

illustrated in figure 4.2. It should be noted that, as shown in [GZ], there exists four-row planar layout instances that are not three-layer wirable. Hence, it is impossible to construct a four-row layer assignment algorithm for arbitrary planar layouts.

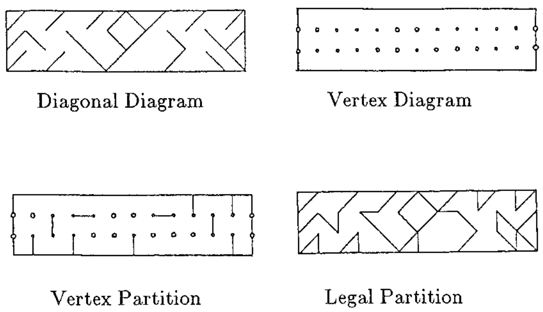


figure 4.2

V. A LAYER ASSIGNMENT ALGORITHM FOR A CLASS OF FOUR-ROW PLANAR LAYOUTS.

In this section we present an algorithm to construct a legal partition for any four-row diagonal diagram of degree 1. There are three internal grid lines in G(R). Assign the y-coordinate one to the upper internal grid line, three to the middle internal grid line, and two to the lower internal grid line (this ordering facilitates the proof of correctness). Assign the x-coordinate zero to the left boundary of G(R), one to the vertical grid line (column) immediate to the right of the left boundary of G(R), and so on. Each vertex in the diagonal diagram of degree one will be represented by its location on the grid. Sort the vertices of D into an ordered list $v_1 = (x_1, y_1)$, $v_2 = (x_2, y_2)$, ..., $v_q = (x_q, y_q)$ such that $x_i \leq x_{i+1}$ and if $x_i = x_{i+1}$, $y_i > y_{i+1}$. The vertices will be referred as *top, middle* or *bottom,* depending on which internal grid line in G(R) they are located. Since the diagonal diagrams are of degree 1, any legal partition is a collection of vertex disjoint alternating paths and cycles composed of lines and diagonals. In the final legal partition every vertex has exactly one vertical or horizontal partitioning line incident to it. After adding a set of partitioning line segments to a diagonal diagram we say that it forms a *partial legal partition* if there are no forbidden patterns and every vertex has either one diagonal, or a diagonal and a vertical or horizontal line segment incident to it. Unlike procedure 3ROW_ASSIGN, connections cannot be made by only concentrating on the structure of vertex diagram and totally ignoring the diagonals. When the number of rows in the layout is greater than three, it seems unlikely that one can construct a legal partition in a left-to-right column by column fashion.

Our algorithm, 4ROW-ASSIGN, consists of three procedures: VERTICAL, MODIFY and HORIZONTAL. These procedures are invoked as follows. At each step we have a partial partition and we find the smallest positive integer c such that vertex v_c not connected by a partioning line segment. Then our procedures construct a partial partition such that vertices v_1, v_2, ..., v_c and possibly other vertices have a partitioning line segment incident to it. The first step invokes procedure VERTICAL. If procedure VERTICAL fails to make a vertical connection for v_c, procedure MODIFY will perform the connection by modifying some previously made connections as well as performing all connections for the vertices in the current column x_c. Whenever procedure MODIFY introduces a horizontal line segment to the right of the current column, x_c, procedure HORIZONTAL completes the connections of the vertices above and below this horizontal line segment. At this point we select another vertex v_c with the above properties. This process continues until all vertices are connected by exactly one partitioning line and the entire configuration is a legal partition. For brevity we will not discuss these procedures in more detail. Interested readers can find these procedures in [GZ1].

Theorem 5.1: Algorithm 4ROW-ASSIGN generates a three-layer assignment for any four-row planar layout in O(n) time, where n is the number of columns in R.
Proof: For brevity the proof is omitted.

□

VI. DISCUSSION.

As we mentioned in section I, the idea of stretching a planar layout to make it wirable in less than four layers is not new. In [MP] it is shown that by inserting an empty track between every two adjacent tracks of R any planar layout is two-layer wirable. In fact, this idea can be traced back to the paper [RBM] where the channel routing problem is considered. In contrast to the previous methods, the approach in [GZ1] tries to reduce the additional wiring area as much as possible. To achieve this, they give a stretching scheme that given certain planar layout structures and algorithms, it explores the best possible stretchings that allow a three-layer wiring. This scheme has the advantage that if a planar layout has only a few sublayouts with complex structures, it can be wired by taking this information into account. To take advantage of this approach, it is necessary to classify layouts according to their structure.

Gonzalez and Zheng [GZ] propose a classification of planar layouts. They classify planar layouts into four classes depending on the properties of their diagonal diagram. It turns out that these classes form an interesting hierarchy. They show that these layout classes have different wirability properties. For example, they show that there exist four-row planar layouts in the general layout class and seven-row planar layouts in the simplest layout class that are not three-layer wirable. By using their wirability results they give lower bounds for best possible approximation bounds for our stretching strategy.

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